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Limit Cycles in a Ternary Structure

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Abstract

The limit cycle behavior of a ternary filtering structure is investigated. It is found that the limit cycles behavior is dependent on the initial conditions of quantization error and the gain parameter in addition to the level of the dc input. The system is simulated and a random search procedure is set up to explore and extract its cyclical patterns.

1. Introduction

One of the ill-understood behavior patterns of \( \Sigma \Delta \) modulators is the generation of periodic patterns or limit cycles at its output. Such a cyclic output produces discrete noise components. Remarkable studies have been made on the limit cycle nature of the first- and second-order \( \Sigma \Delta \) modulators and on their elimination \[1\]-\[3\]. Despite the numerous attempts to identify the limit cycle mode of higher order (more than 2) \( \Sigma \Delta \) systems \[4\], an exact analysis has not been achieved yet. Understanding the limit cycle phenomenon in these systems is becoming more demanding due to their improved performance at equivalent oversampling ratios, which make them attractive to \( \Sigma \Delta \) system designers. Moreover, due to their instability problem, which is the main drawback in these topologies, the limit cycle behavior should be thoroughly investigated as it has a strong relation to the issue of instability \[5\].

In this paper we attempted to conduct a comprehensive analysis to the ternary-\( \Sigma \Delta \) topology, which is regarded as a third order \( \Sigma \Delta \) modulator, both mathematically and by simulation.

2. System Analysis

The ternary structure in Fig.(1), which was utilized by \[6\]-\[7\]-\[8]\-[9] to design single-bit DSP systems, is basically a third-order IIR filter. To analyze this system, let as assume \( x \) as the dc input, \( u(k) \) is the integrator output (just precede the quantizer), and then the quantizer output, \( y(k) \) will be given by: \( y(k) = \text{sgn}[u(k)] \).

![Figure 1. Single-bit ternary filter.](image1)

![Figure 2. Single-bit second-order SD filter.](image2)
This system can be described as follows:

\[ u(k) = 3u(k-1) - 3u(k-2) + u(k-3) \]
\[ -(\alpha + 2)y(k-1) + 3y(k-2) - y(k-3) + x. \]  
(1)

where \( \alpha \) is a constant parameter. The complete iterative solution to eqn(1) is:

\[ u(k) = \left( \frac{1}{2} \right) k(k-1)u_2 - k(k-2)u_1 + p(k)u_o \]
\[ -p(k)y_o + k(k-2)y_1 - (k-1)y_2 - \alpha p(k)y_2 \]
\[ -g(k,\alpha) + d(k)x. \]  
(2)

where \( u_o, u_1, \) and \( u_2 \) are the initial values of the integrator output, and \( y_i = \text{sgn}(u_i). \) The functions \( p(n), g(n), \) and \( d(n) \) are given as follows:

\[ p(k) = (k-1)(k-2)/2 \]
(3)

\[ g(k,\alpha) = \sum_{n=1}^{k-3} \left( \left( \frac{1}{2} \right) n(n+1)\alpha + n + 1 \right) y(k-n) \]  
(4)

\[ d(k) = kp(k)/3. \]  
(5)

If \( \alpha = 1, \) eqn.(2) becomes:

\[ u(k) = \frac{1}{2} k(k-1)e_2 - k(k-2)e_1 + p(k)e_o - \hat{g}(k) + d(k)x, \]  
(6)

where \( e_i = u_i - \text{sgn}(u_i), \) whereas \( \hat{g}(k) \) represents the case when \( \alpha = 1 \) and is given by:

\[ \hat{g}(k) = g(k,1) = \frac{1}{2} \sum_{n=1}^{k-3} \left[ \left( n + 2 \right) (n + 1) \right] y(k-n). \]  
(7)

If we assume a limit cycle of length \( L \) has occurred in the system, then from eqn.(2), \( y(k + L) = y(k). \) Solving and arranging for \( L \) yields:

\[ -L^2 \left( u_2 - \alpha y_2 - 2e_1 + e_o \right) \]
\[ + \frac{L}{2} \left( u_2 + (2 - 3\alpha)y_2 - 4e_1 + 3e_o \right) \]
\[ -kL(u_2 - \alpha y_2 - 2e_1 + e_o) - (g(k,\alpha) - g(k + L,\alpha)) \]
\[ = (d(k + L) - d(k))x. \]  
(8)

If \( \alpha = 1, \) then \( u_2 - \alpha y_2 = u_2 + (2 - 3\alpha)y_2 = e_2, \) and eqn.(8) becomes:

\[ -L^2 \left( e_2 - 2e_1 + e_o \right) + \frac{L}{2} \left( e_2 - 4e_1 + 3e_o \right) \]
\[ -kL(e_2 - 2e_1 + e_o) - \hat{g}(k) - \hat{g}(k + L) \]
\[ = (d(k + L) - d(k))x. \]  
(9)

It is evident from eqn.(8) that the gain parameter has an important role in this matter, as it affects the initial conditions as well as the steady state operation. Both eqn.(8) and eqn.(9) imply that the occurrence of limit cycles in this structure is conditional. If we adopt the approach in [10][11], by assuming \( x \) to belong to the set of rational numbers \( a/b, \) where \( a \) and \( b \) are prime integers, then all the terms that contain the signum function and multiplied by integer factors are also a subset of the same set of rational numbers, \( a/b. \) However, this condition is not sufficient in our structure to produce limit cycles and another condition should be met as well. Specifically, in eqn.(8) the factor \( (u_2 - \alpha y_2 - 2e_1 + e_o) \) or the factor \( (e_2 - 2e_1 + e_o) \) in eqn.(9) must be equal to zero. Therefore, limit cycles occur in the ternary-\( \Sigma \Delta \) system with periods of \( L \) given by:

\[ L = \frac{(b_{k+L} - b_k)}{a(u_2 - (2 - 3\alpha)y_2 - 4u_1 + 3u_o)}. \]  
(10)

### 3 Limit Cycles: Analysis and Simulation

In this section we focus on the detection and extraction of the limit cycles at the system output. This is done in both the frequency domain (using FFT) and time domain (using autocorrelation). The effect of OSR (oversampling ratio) will also be considered.

The cyclic sequences will be described as follows [12]:

\[ Q(i,j) = [+q_1, -q_1, ... + q_{i-1}, -q_{i-1}, +q_i, -q_i] \]

where \( i \) denotes the number of transitions from +1 to -1 (or -1 to +1) within the limit cycle period, while the subscript \( j \) represents any integer. The values between brackets represent successive outputs that constitute one cycle, where \(+q_i\) represents the number of consecutive +1’s, whereas \(-q_i\) represents the number of consecutive -1’s, both at the \( i^{th} \) transition.

#### 3.1 Zero-Input Limit Cycles

Fig.(3) illustrates an approach to find periodic patterns in the ternary structure. A sufficiently large number of lags (clock periods) in the autocorrelation function, \( R_{xy}(n) \), should be used to insure that no longer cyclic period does exist. The figure reveals that the maximum limit cycle length \( L_{\text{max}} \) for zero input in the ternary-\( \Sigma \Delta \) topology shown in Fig.(1) is \( L_{\text{max}} = 8. \) Same result can be obtained from the frequency domain, whereby the fundamental limit cycle frequency \( f_o \) and its harmonics are located and then \( L_{\text{max}} \) can be calculated as follows:

\[ L_{\text{max}} = f_s/f_o. \]  
(11)

where \( f_s \) is the sampling frequency. However, one should be aware that this is true only for stationary signals. Furthermore, the number of transitions \( i \) within the limit cycle is calculated as shown in Fig.(4), where it is obvious that
3.2 Limit Cycles for DC Inputs

The ternary-$\Sigma\Delta$ filter exhibits a highly non-linear limit cycle behavior. Furthermore, the parameter $\alpha$ appends an extra variable to the problem. On one hand, $\alpha$ controls the maximum dc input $x_{max}$ beyond which no limit cycle can be detected. This can be seen in Fig.(6). On the other hand, as anticipated by eqn.(8), $\alpha$ may alter the limit cycle behavior through the variation of both the initial and steady-state conditions of the system. This alteration extends to include the quantization noise structure as well.

The frequencies of these patterns normally reside in the baseband region, however, their power is relatively low. This is due to the noise shaping effect of the $\Sigma\Delta$ modulator in this band of frequency. Shorter cycles that are in fact subsets of $L_{max}$ (and consequently located in a higher frequency band) suffer several orders of magnitude less attenuation, and therefore aggravate the problem of instability. As an example in this simulation: at $x=1/20$, Fig.(7) depicts the
Although it is difficult to predict $L_{\star}$ which is basically a third-order and second-order version of $\Sigma \Delta$ modulator possesses a highly non-linear behavior and seemed that this topology, which is similar to third order and extract the limit cycles and identify their features. It\'s extensively and a random search method is utilized to discover dc input magnitude. The system was then simulated extensively and a random search method is utilized to discover and extract the limit cycles and identify their features. It seemed that this topology, which is similar to third order $\Sigma \Delta$ modulator possesses a highly non-linear behavior and is similar in some aspects to that of the first and second order $\Sigma \Delta$ modulators. Further insight investigation is recommended, as the issue of limit cycles in higher order modulators is vital for instability problem.

4 Conclusions

A ternary-$\Sigma \Delta$ structure was analyzed mathematically without imposing any approximations. It was evident that the system exhibits a conditional limit cycle behavior. These conditions includes the initial quantization noise conditions and the constant gain parameter in addition to the dc input magnitude. The system was then simulated extensively and a random search method is utilized to discover and extract the limit cycles and identify their features. It seemed that this topology, which is similar to third order $\Sigma \Delta$ modulator possesses a highly non-linear behavior and is similar in some aspects to that of the first and second order $\Sigma \Delta$ modulators. Further insight investigation is recommended, as the issue of limit cycles in higher order modulators is vital for instability problem.

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